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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,220	05/09/2001	Shunpei Yamazaki	SEL 259	4950

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EXAMINER	
ABDULSELAM, ABBAS I	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/852,220	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Abbas I. Abdulselam	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-10,12-21,23-25,27-29,31-33,35-37,40,41,43 and 45-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-10,12-21,23-25,27-29,31-33,35-37,40,41,43 and 45-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to a communication filed on 11/30/06. Claims *1-4,6-10,12-21,23-25,27-29,31-33,35-37,40,41,43 and 45-69* are pending and claims 5, 11, 22, 26, 30, 34, 38-39, 42 and 44 are canceled

Response to Arguments

2. Applicant's arguments filed on 11/30/06 have been fully considered but they are not persuasive.

Applicant argues the cited references, Masuda et al. (USPN 6107983) and (USPN 4644338) alone or in combination do not teach light emitting device in which all semiconductor elements in a display portion and a driver circuit are n-channel type semiconductor elements.

However as shown in the art rejection below, Aoki teaches a liquid crystal display system as shown in Fig. 5 in which the peripheral circuits for driving the semiconductor driver elements are formed on the surface of the substrate on which the thin-film transistors 6R, 6G, 6B for driving the liquid crystal are fabricated. More specifically, Aoki teaches the latch circuit 26 serving as the column driver and the shift register 29 are fabricated as integrated circuits on the substrate 12, and the gate line selector and driver circuit 32 is fabricated as an integrated circuit on the substrate. Aoki shows that the peripheral circuits 26, 29, 32 can be formed simultaneously with the thin-film transistors 6R, 6G, 6B on the substrate 12 without having to increase the number of fabrication steps required (col. 7, lines 29-51).

Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Masuda's liquid crystal display system shown in Fig. 2 to adapt Aoki's simultaneous formation of peripheral circuit with thin film transistors as illustrated in Fig.

5 because simultaneous formation of peripheral circuit with thin film transistors helps a liquid crystal display to selectively drive in order that a variety of displaying pattern is achieved (col. 5, lines 9). Note that Masuda also teaches the use of various types of display devices including with variable light emitting capabilities (col. 15, lines 32-40).

Hence, Aoki's teaching reads over the argued claim limitation.

Applicant argues with respect to claim 7, the cited references do not teach a switching element a current control element. However, Masuda teaches as shown in Fig. 7 a plurality of switches 343a, and Aoki teaches fabrication of a thin-film transistor with respect to application of current (col. 10, lines 35-37).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 6-10, 12-18 and 52-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda et al. (USPN 6107983) in view Aoki et al. (USPN 4644338).

Regarding claims 1, 7 and 13, Masuda teaches a liquid crystal display device (101) with a substrate (111), which includes driver circuits (210a, 201b, 301a, 301b), and a plurality of thin film transistors, TFTs (165) coupled with pixel electrodes (col. 5, lines 28-46 and Fig. 2 (210a, 201b, 301a, 301b)). Masuda also teaches that the driving circuit (201a) includes a logic circuit section (215a), which in turn includes two 2-input NAND gates NA1 and NA2 (col. 6, lines 34-45 and Fig. 3 (NAND)). Furthermore, Masuda points out the use of a decoder having a plurality of logic circuits (col. 1, lines 60-67 and col. 2, lines 1-5). Masuda teaches the use of various types of liquid crystal display device including a display device with an element of light modulation, and a display element with variable light emitting capabilities (col. 15, lines 32-4).

However, Masuda does not teach all semiconductor elements in the display portion and the driver circuit are n-channel type semiconductor elements.

Aoki on the other hand teaches a liquid crystal display system as shown in Fig. 5 in which the peripheral circuits for driving the semiconductor driver elements are formed on the surface of the substrate on which the thin-film transistors 6R, 6G, 6B for driving the liquid crystal are fabricated. More specifically, Aoki teaches the latch circuit 26 serving as the column driver and the shift register 29 are fabricated as integrated circuits on the substrate 12, and the gate line selector and driver circuit 32 is fabricated as an integrated circuit on the substrate. Aoki shows that the peripheral circuits 26, 29, 32 can be formed simultaneously with the thin-film transistors 6R, 6G, 6B on the substrate 12 without having to increase the number of fabrication steps required (col. 7, lines 29-51).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Masuda's liquid crystal display system shown in Fig. 2 to adapt

Aoki's simultaneous formation of peripheral circuit with thin film transistors as illustrated in Fig. 5 because simultaneous formation of peripheral circuit with thin film transistors helps a liquid crystal display to selectively drive in order that a variety of displaying pattern is achieved (col. 5, lines 9).

Note that Masuda also teaches the use of various types of display devices including with variable light emitting capabilities (col. 15, lines 32-40).

Regarding claims 4, 10 and 14, Aoki illustrates as shown in Fig. 10 is a block diagram of a driver circuit for the liquid crystal display. It would have been obvious to utilize the desired type transistors in a desired configuration.

Regarding claims 2, 8 and 15, Masuda teaches the use of a substrate (Fig. 2 (111) and col. 5, lines 28-46). Aoki also teaches the substrates 12, 13, which may be formed of high polymers such as polyimide or fluorine plastics (col. 8, lines 35-36).

Regarding claims 3, 9 and 16, Masuda teaches the use of TFT (165) (Fig. 2 (165) and col. 30-46).

Regarding claims 6, 12, and 17-18, Masuda teaches the use of the liquid crystal projector 1 with three liquid crystal display devices 101, 501 and 601 (col. 4, lines 1-67 and col. 5, lines 1-13).

Regarding claim 52-54, Aoki teaches that the semiconductor layer is subjected to photoetching to form a semiconductor silicon layer 24 or channel region extending between and

deposited on edges of the drain and source electrodes 25, 3, as illustrated in FIG. 15 (col. 9, lines 27-31)

5. Claims 19-21, 23-25, 27-29, 31-33, 35-37, 40-41, 43, 45-51 and 55-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda et al. in view of Aoki et al. and Tsutsumi et al. (USPN 6713748).

Regarding claims 19, 24, 28, 32, 36 and 41, Masuda teaches a liquid crystal display device (101) with a substrate (111), which includes driver circuits (210a, 201b, 301a, 301b), and a plurality of thin film transistors, TFTs (165) coupled with pixel electrodes (col. 5, lines 28-46 and Fig. 2 (210a, 201b, 301a, 301b)). Masuda also teaches that the driving circuit (201a) includes a logic circuit section (215a), which in turn includes two 2-input NAND gates NA1 and NA2 (col. 6, lines 34-45 and Fig. 3 (NAND)). Furthermore, Masuda points out the use of a decoder having a plurality of logic circuits (col. 1, lines 60-67 and col. 2, lines 1-5). Masuda teaches the use of various types of liquid crystal display device including a display device with an element of light modulation, and a display element with variable light emitting capabilities (col. 15, lines 32-4). In addition, Masuda teaches either one of the scanning line drive circuits 201a, 201b and video signal line drive circuits 301a, 301b or, one of sets of drive circuits 201a, 201b and 301a, 301b is constructed of a plurality of stages of shift registers (col. 5, lines 28-46).

However, Masuda does not teach all semiconductor elements in the buffer circuit are n-channel type semiconductor elements.

Aoki on the other hand teaches a liquid crystal display system as shown in Fig. 5 in which the peripheral circuits for driving the semiconductor driver elements are formed on the surface of the substrate on which the thin-film transistors 6R, 6G, 6B for driving the liquid crystal are fabricated. More specifically, Aoki teaches the latch circuit 26 serving as the column driver and the shift register 29 are fabricated as integrated circuits on the substrate 12, and the gate line selector and driver circuit 32 is fabricated as an integrated circuit on the substrate. Aoki shows that the peripheral circuits 26, 29, 32 can be formed simultaneously with the thin-film transistors 6R, 6G, 6B on the substrate 12 without having to increase the number of fabrication steps required (col. 7, lines 29-51).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Masuda's liquid crystal display system shown in Fig. 2 to adapt Aoki's simultaneous formation of peripheral circuit with thin film transistors as illustrated in Fig. 5 because simultaneous formation of peripheral circuit with thin film transistors helps a liquid crystal display to selectively drive in order that a variety of displaying pattern is achieved (col. 5, lines 9).

Masuda does not teach first and second semiconductor elements such that a gate of the second semiconductor element is connected to a drain of the first semiconductor element.

Tsutsumi on the other hand discloses as shown in Fig. 8B a circuit in which the gates are connected to the drains of the respective TFTs Tr1 to Trx (col. 10, lines 63-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Masuda's liquid crystal display system shown in Fig. 2 to incorporate Tsutsumi's arrangement of transistors as illustrated in Fig. 8B because the use of transistors helps form planar arrangement of pixels in an image detection device as taught by Tsutsumi.

Regarding claims 20, 25, 29, 33, 37and 43, Masuda teaches a pair of electrode substrates111 and 191 (col. 5, lines 19-26).

Regarding claim 21, Masuda teaches the use of TFT (165) (Fig. 2 (165) and col. 30-46).

Regarding claims 23, 27, 31, 35, 40 and 45, Masuda teaches the use of the liquid crystal projector 1 with three liquid crystal display devices 101, 501 and 601 (col. 14, lines 5-20).

Regarding claims 46-51, Aoki illustrates as shown in Fig. 10 is a block diagram of a driver circuit for the liquid crystal display. It would have been obvious to utilize the desired type of circuit and transistors in a desired configuration.

Regarding claims 55-60, Aoki teaches that the semiconductor layer is subjected to photoetching to form a semiconductor silicon layer 24 or channel region extending between and deposited on edges of the drain and source electrodes 25, 3, as illustrated in FIG. 15 (col. 9, lines 27-31).

Regarding claims, 61-69, Masuda teaches as shown in Fig. 7 a plurality of switches 343a, Aoki teaches fabrication of a thin-film transistor with respect to application of current (col. 10, lines 35-37), and Tsutsumi teaches as shown in Fig. 14 TFT T2 being connected between one end of the capacitor142 and a ground terminal to operate as a protective diode.

Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abbas I. Abdulselam whose telephone number is (571) 272-7685. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abbas abdulselam

Examiner

Art Unit 2629

February 15, 2007

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
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